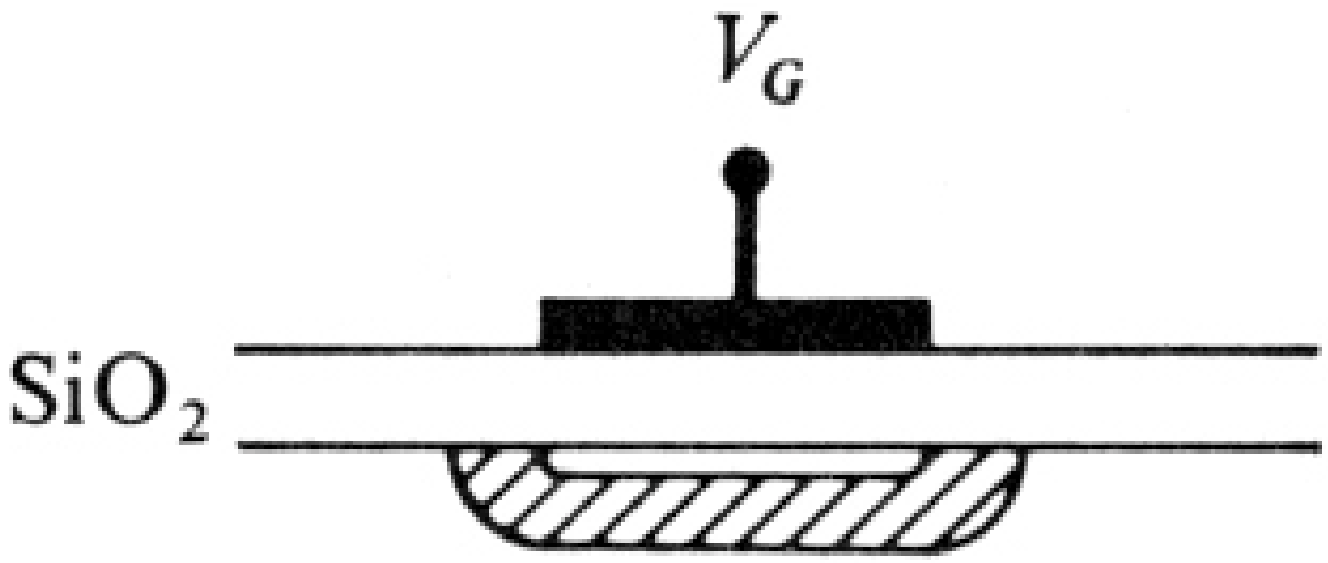
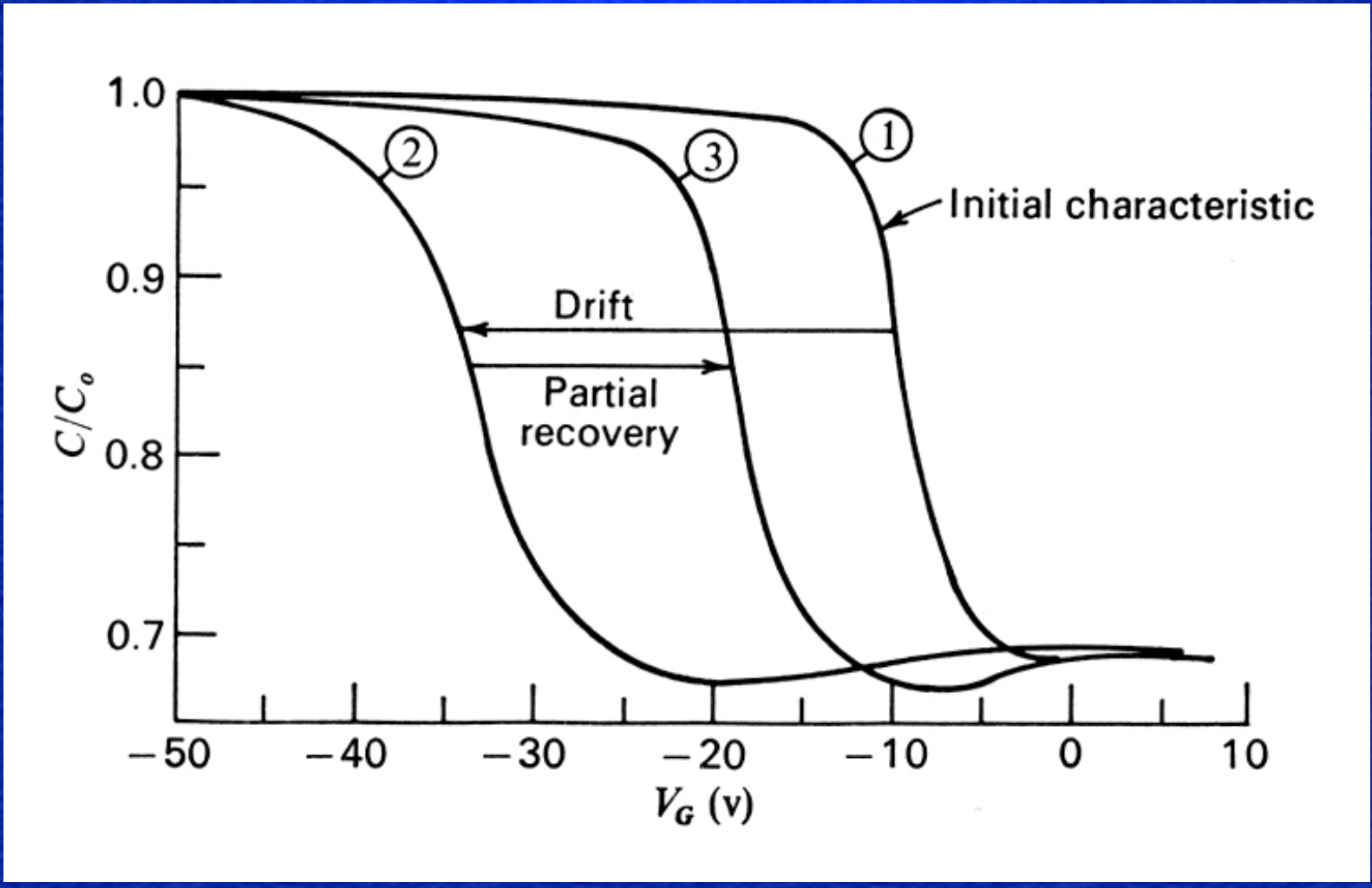
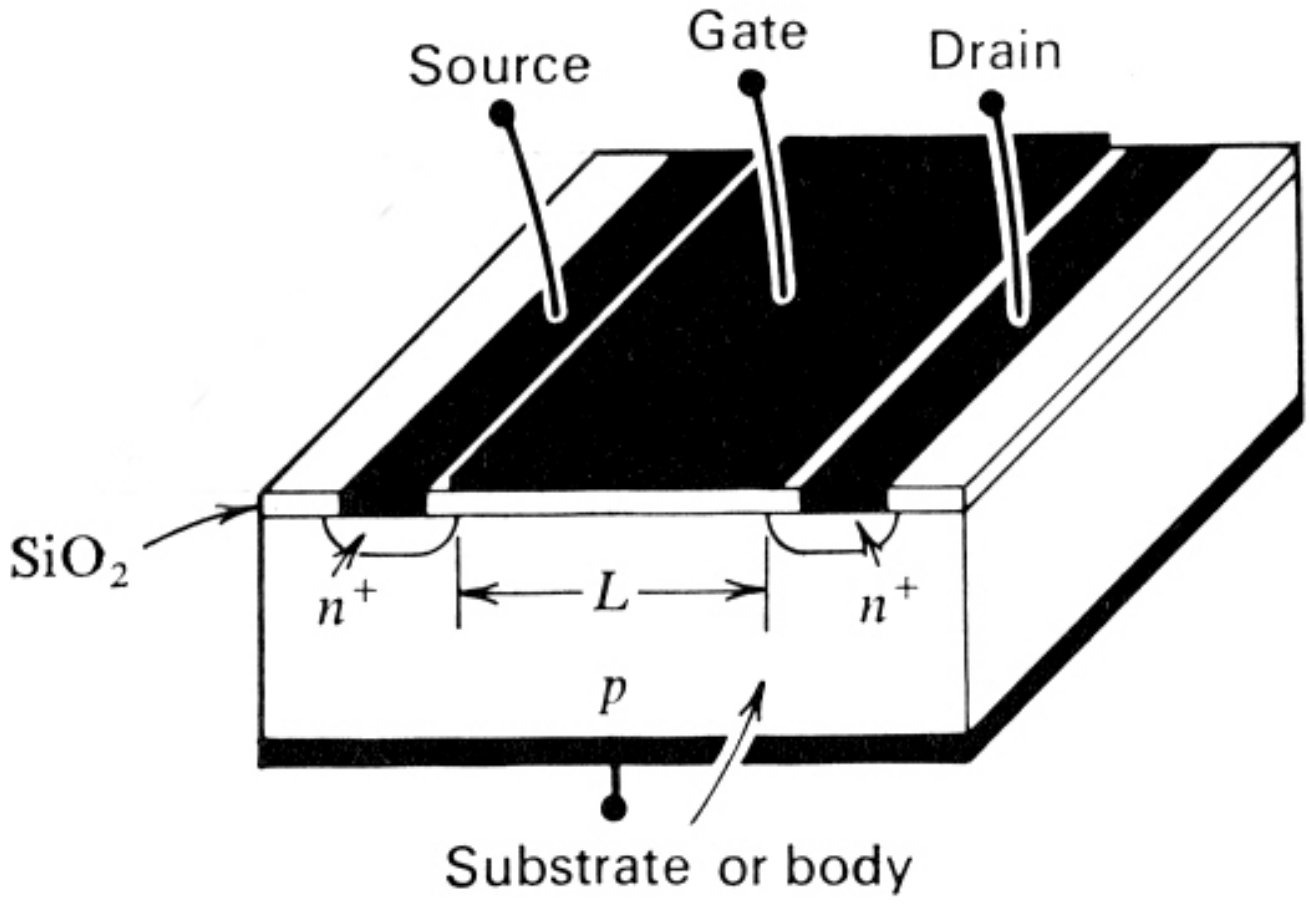
Changing Vectors of Moore's Law

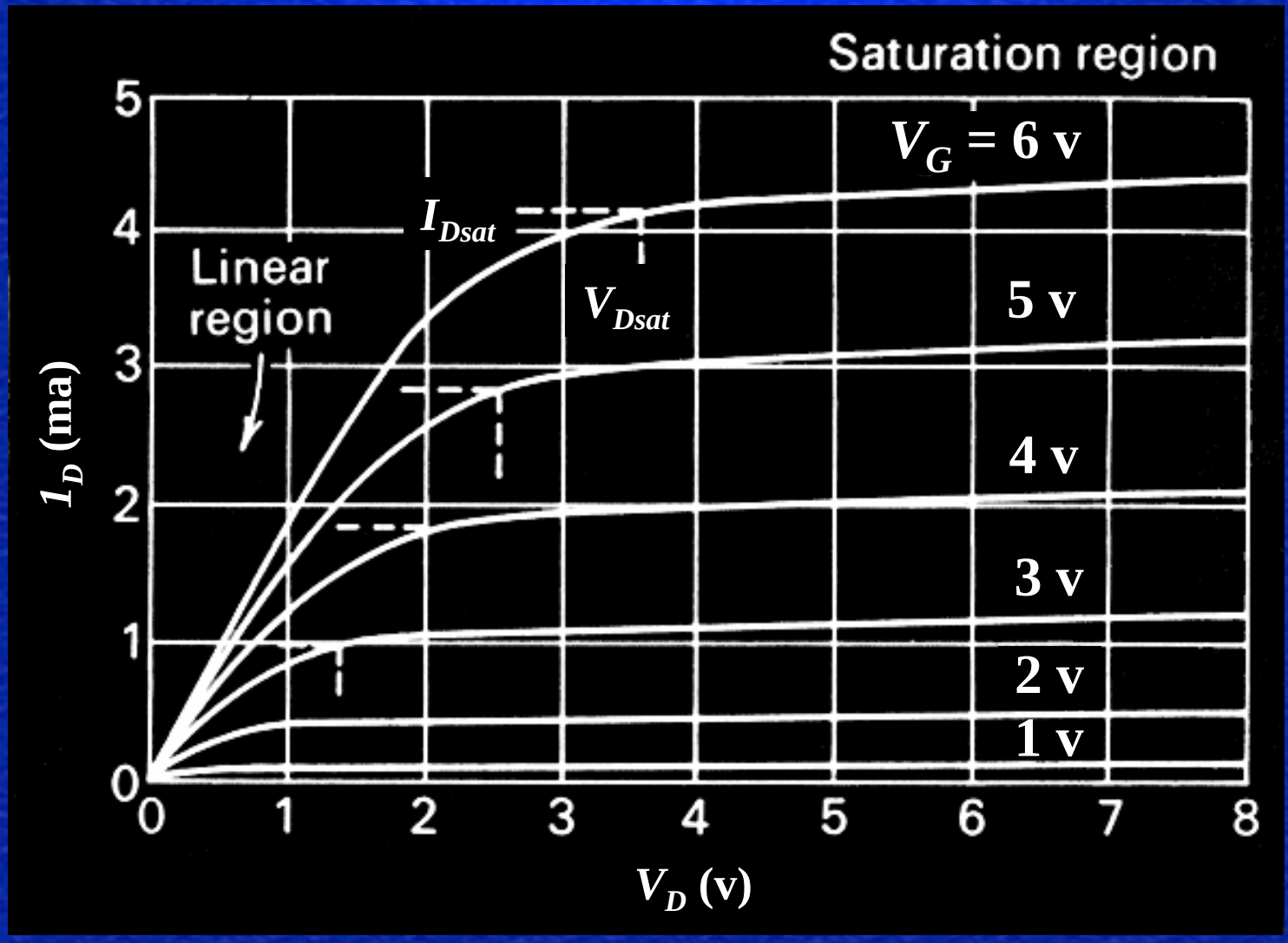
Andy Grove
Chairman of the Board
Intel Corporation

International Electron Devices Meeting
December 10th, 2002


V_G
SiO_2


1.0
0.9
0.8
0.7
C/C_o
1
2
3
Initial characteristic
Drift
Partial
recovery
−50
−40
−30
−20
−10
0
10
V_G (v)


Source
Gate
Drain
SiO_2
n^+
L
n^+
p
Substrate or body


Saturation region
V_G = 6 v
I_{Dsat}
V_{Dsat}
Linear region
5 v
4 v
3 v
2 v
1 v
1_D (ma)
V_D (v)
0
1
2
3
4
5
6
7
8

The Gift of Silicon

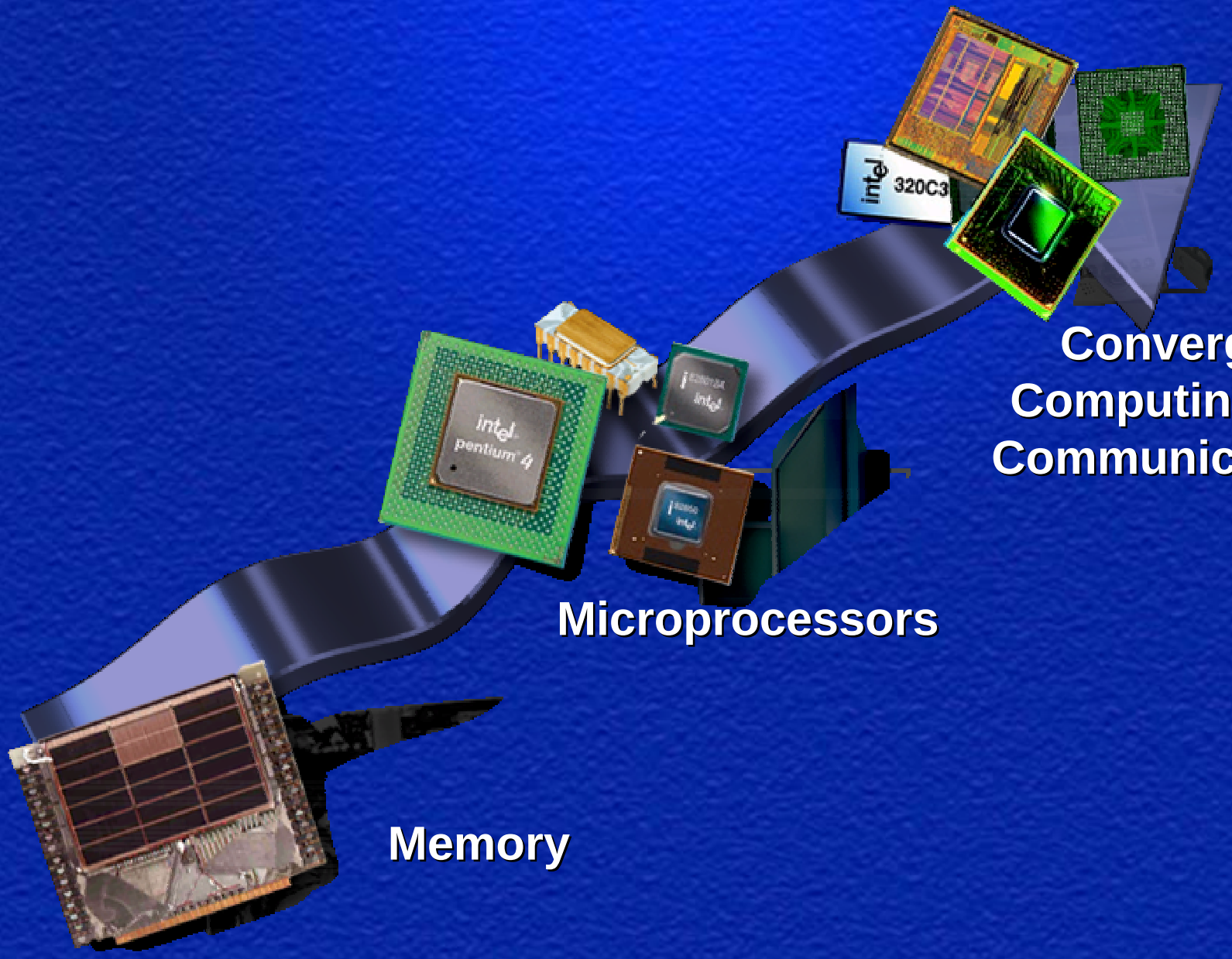
One of the most populous elements

Perfectly mated: Silicon dioxide

Foundation of an industry

Simplicity of MOS transistor fabrication

Silicon is the Engine



Device Integration Gets More Complex

Computational environment spreads

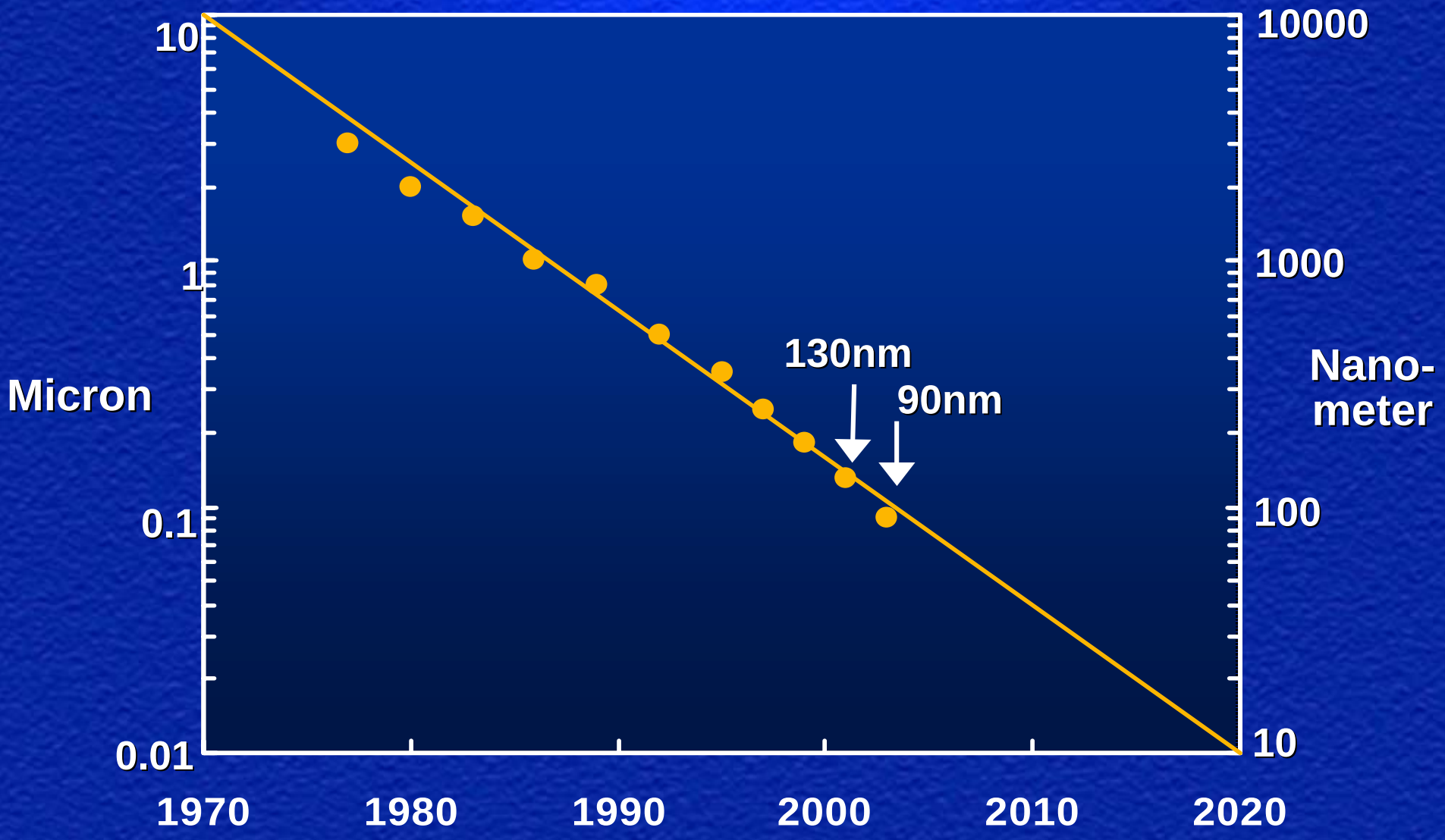
Flash/logic on the same chip

Ubiquitous radios

Nano-scale technology

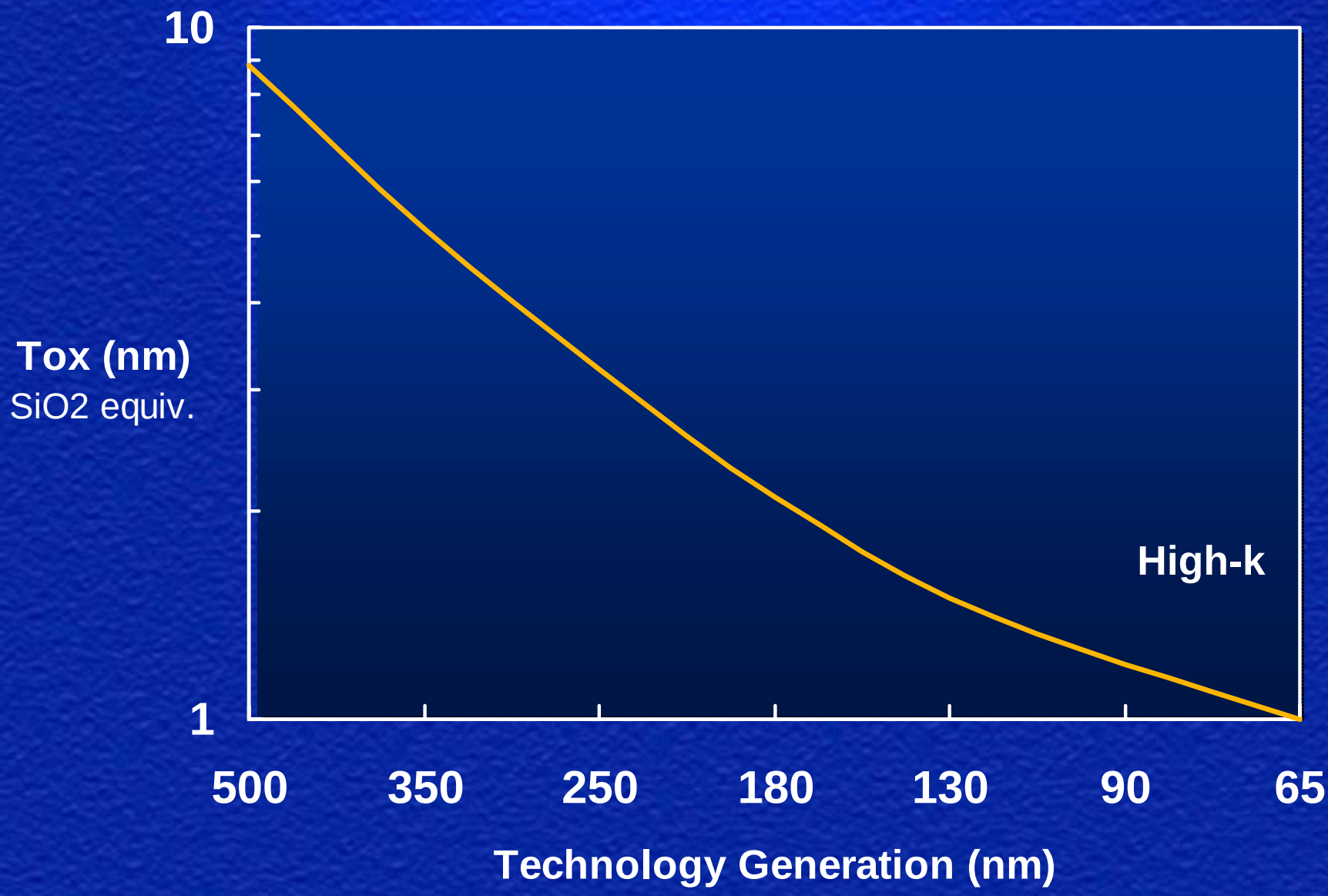
Introduction of new materials

Nominal Feature Size Trends

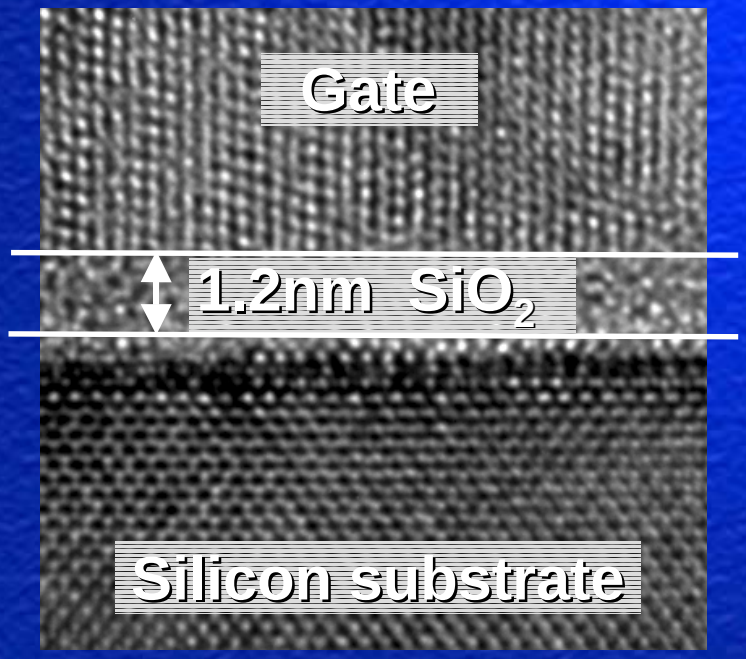


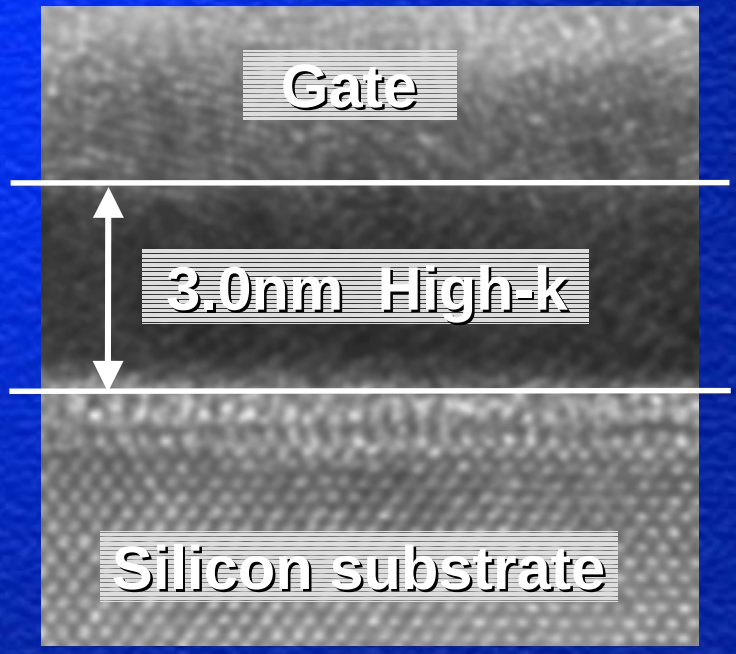
Source: Intel

Gate Oxide Trends



Gate Dielectrics





	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Integration is the key challenge

Source: Intel

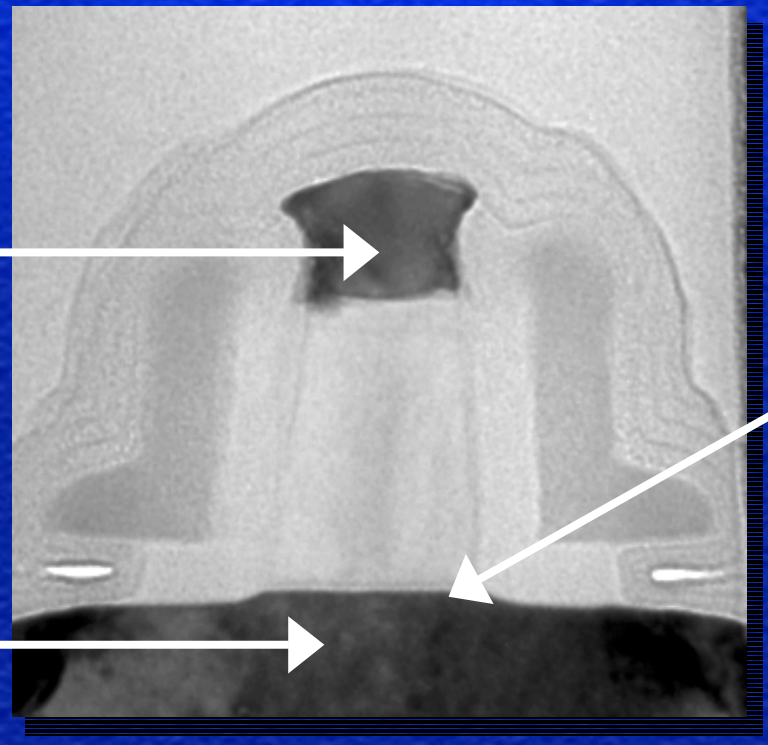
New Materials Extend Si Scaling

Gate

New Silicide material

Channel

Strained silicon

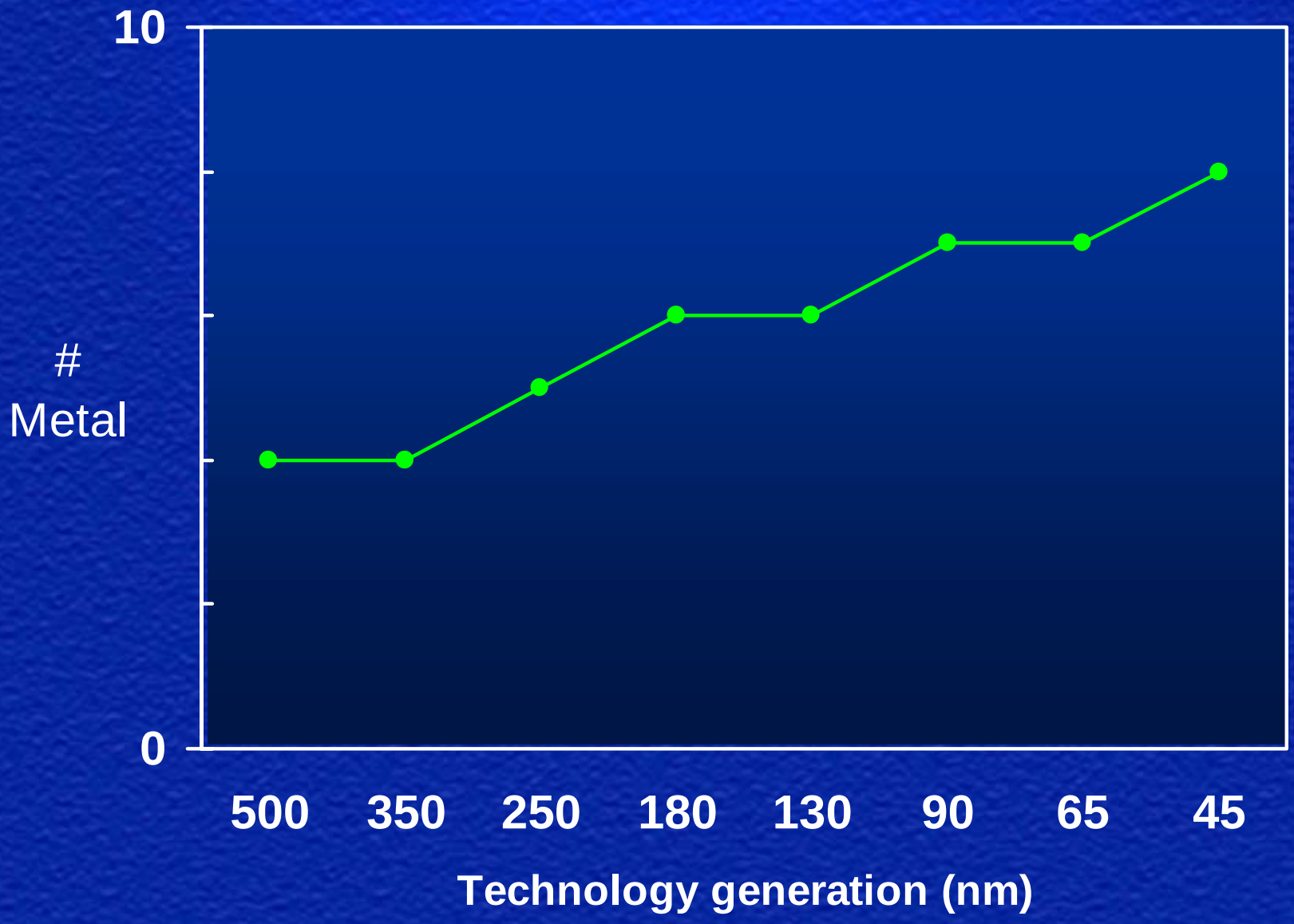


High-k gate dielectric

Transistor

Source: Intel

Interconnect Trends



New Materials for Interconnects

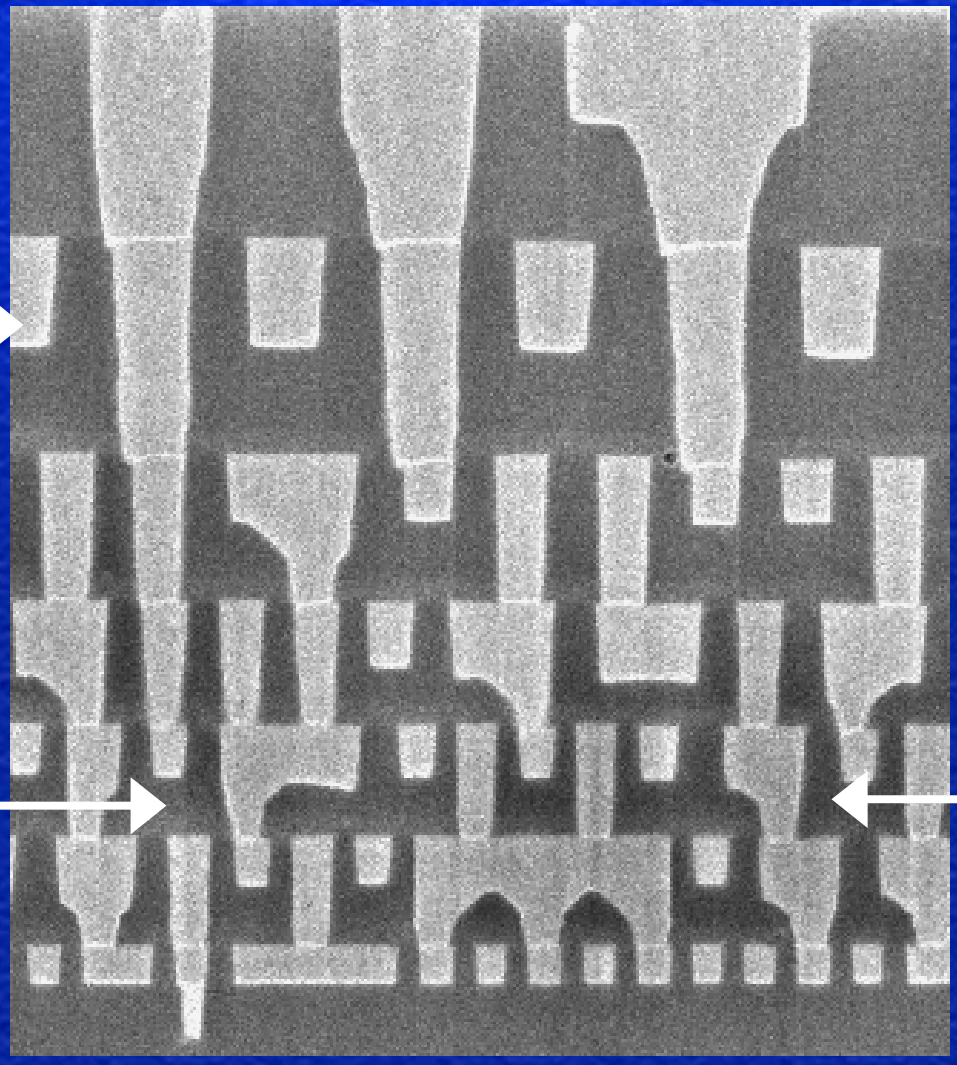
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Interconnects

Future Options

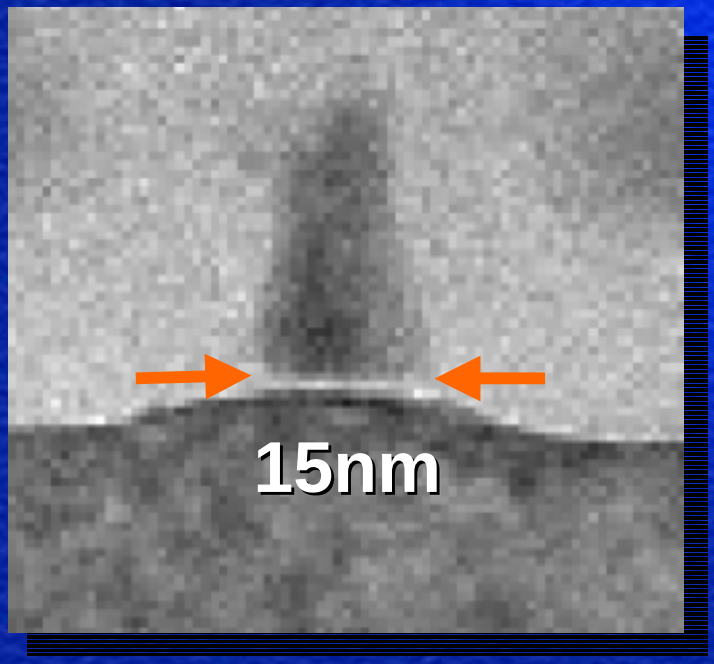
Ultra Low-k Dielectric

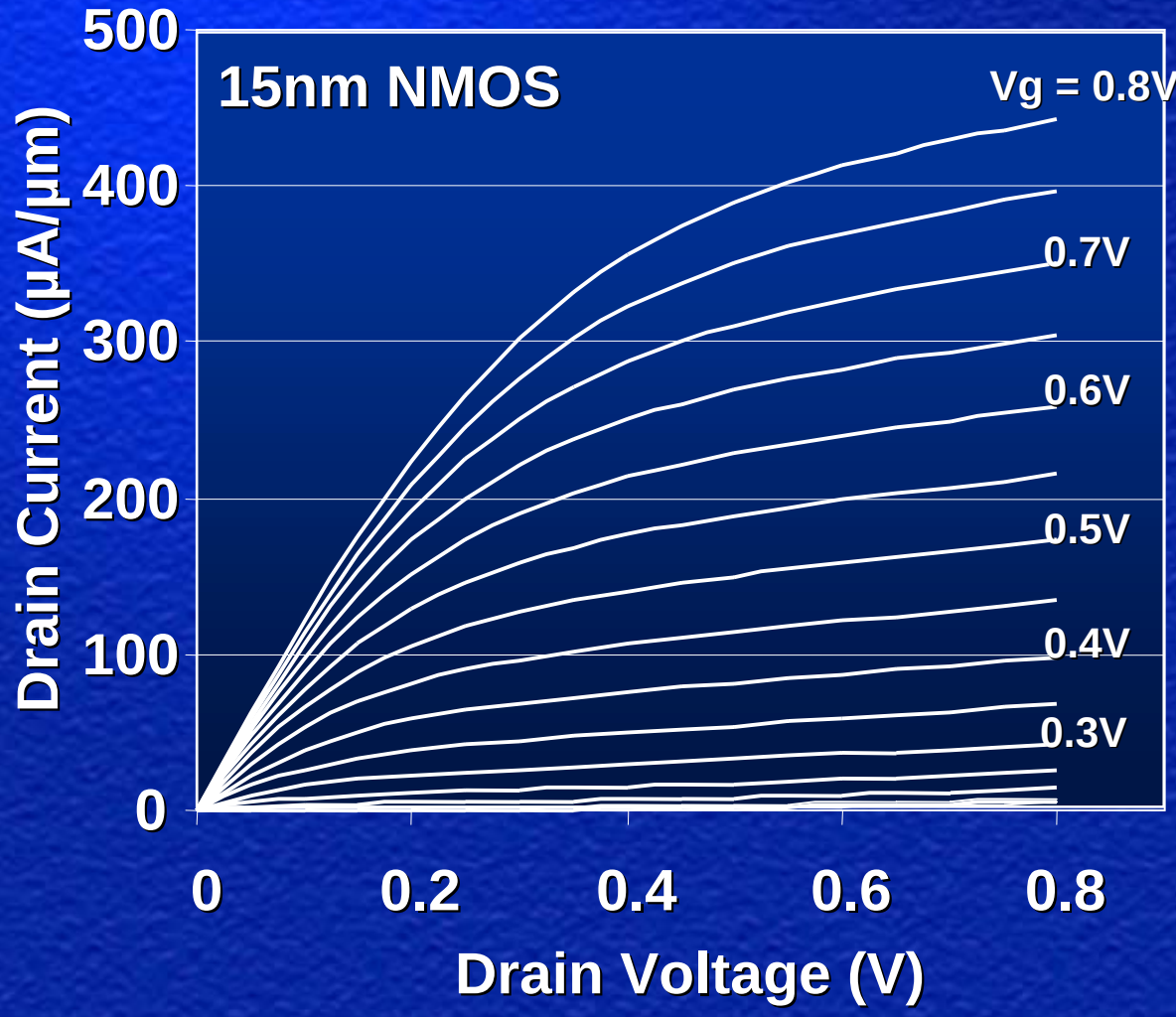
Source: Intel

Number of Materials

Started	Now
~5	~20

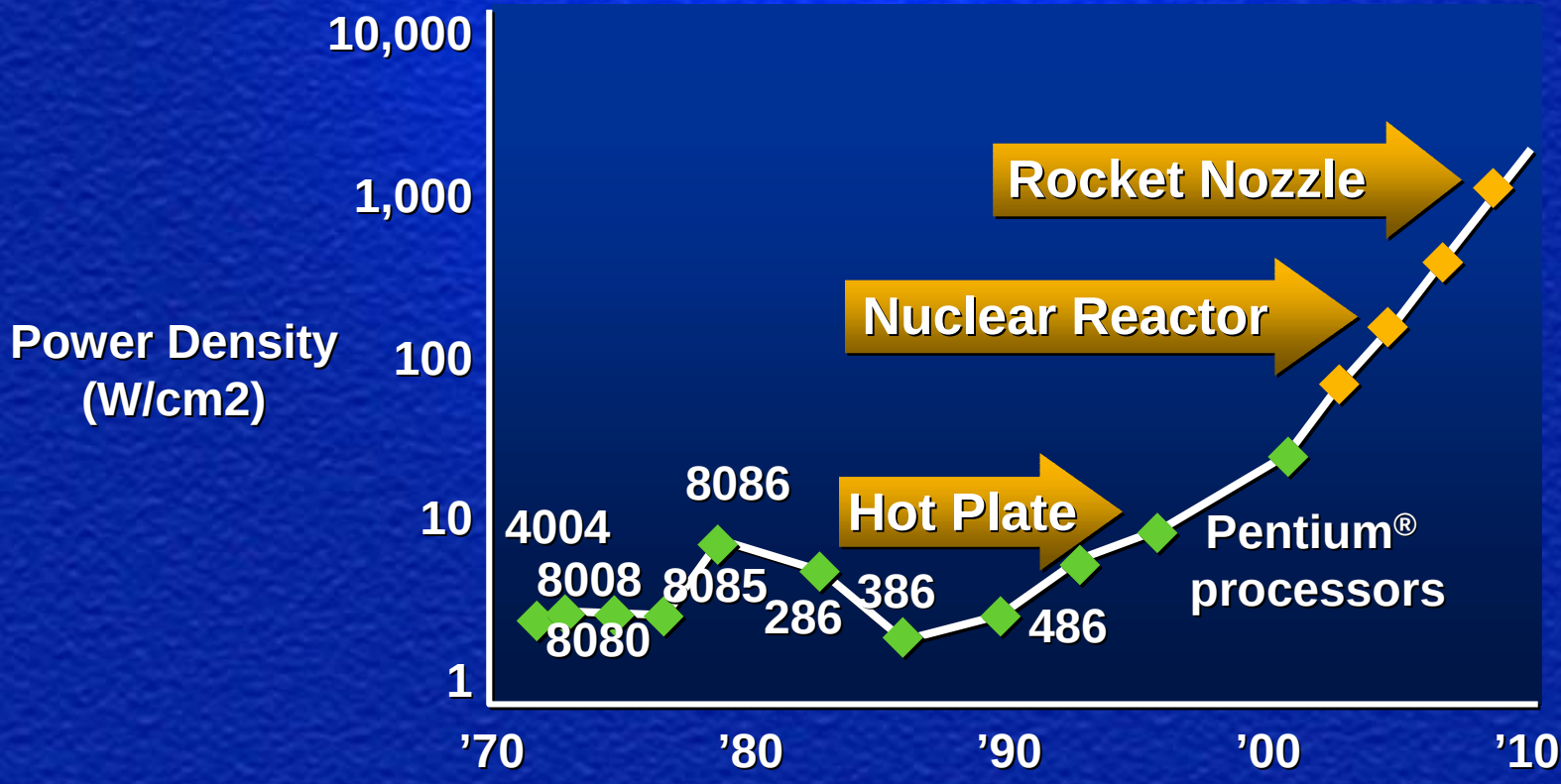
Experimental 15nm Transistor





Problem: High off-current

Power Density Will Get Even Worse

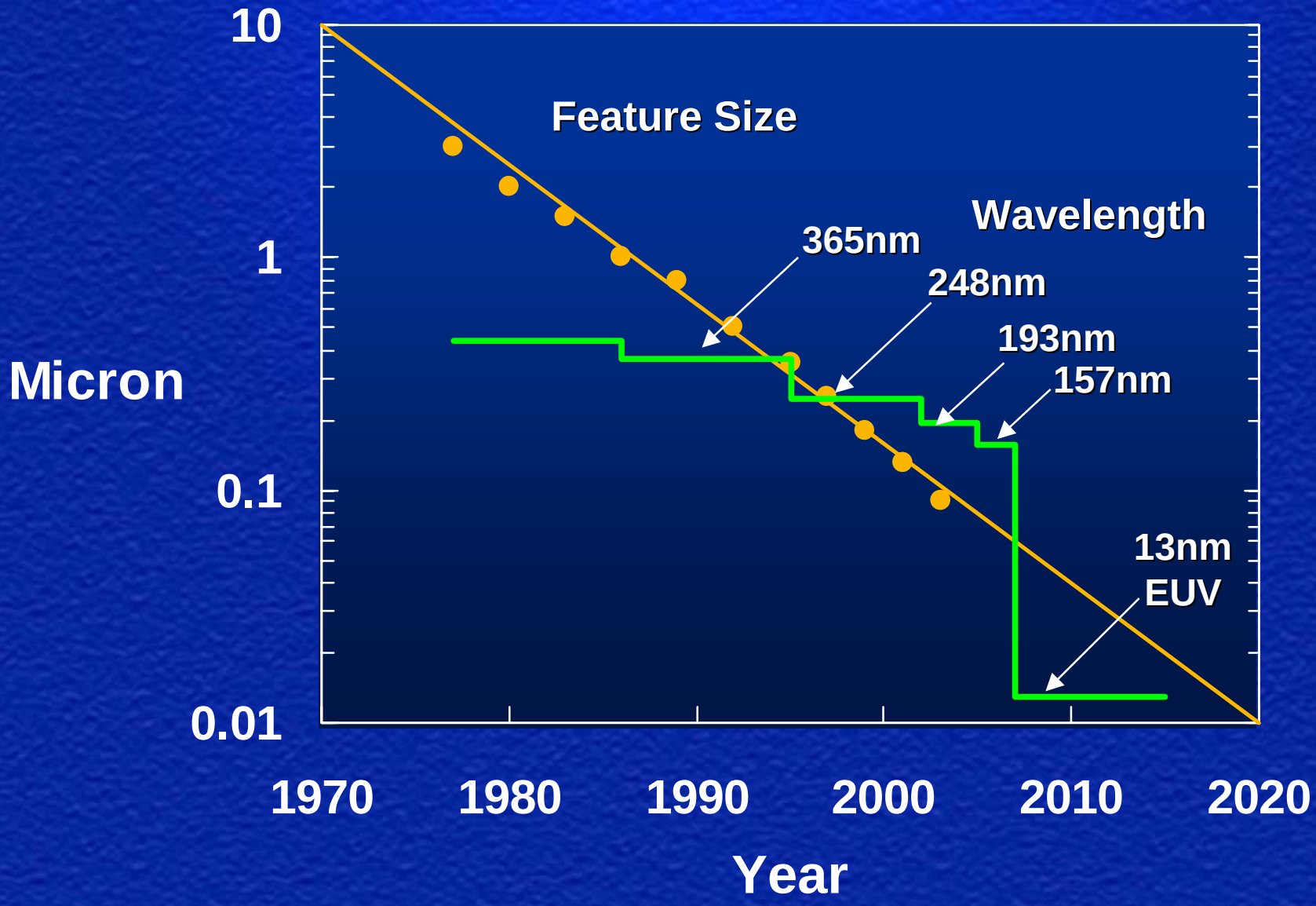


Need to Keep the Junctions Cool

- Performance (Higher Frequency)
- Lower leakage (Exponential)
- Better reliability (Exponential)

Power Trends:
Power Leakage

Lithography Trend



Minimum Economic Scale

Mid 60's	< $1M
Mid 70's	$3M
Early 90's	$1B
'02	$3B
2010	$??B

Continuing traditional scaling:

new (nano) frontier

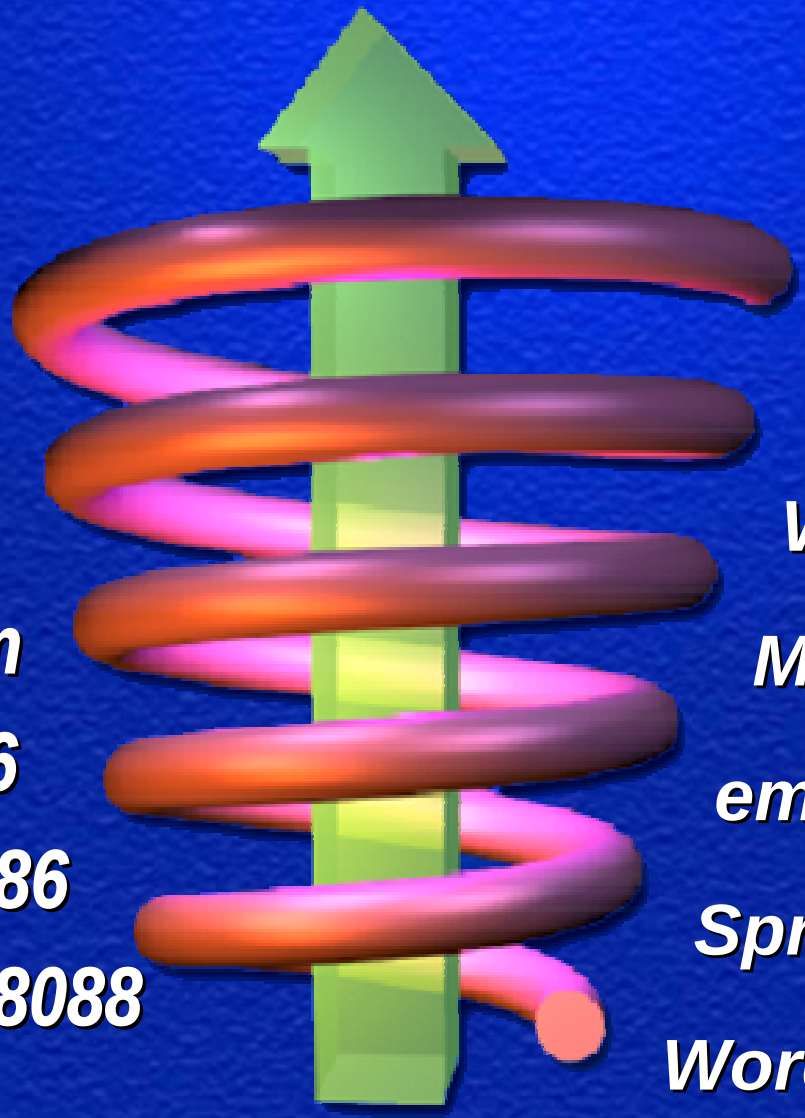
Interconnects: 3rd dimension

Leakage: power limiter!

Transistors & Interconnects: new materials

Cost: minimum economic scale skyrockets

Silicon devices are the foundation of the digital spiral



Pentium 4

Pentium 3

Pentium 2

Pentium

486

386

8088

Killer environment

Digital audio/photo

WWW

Multi-media

email

Spreadsheets

Word processing

The Killer Environment

A complete digital platform

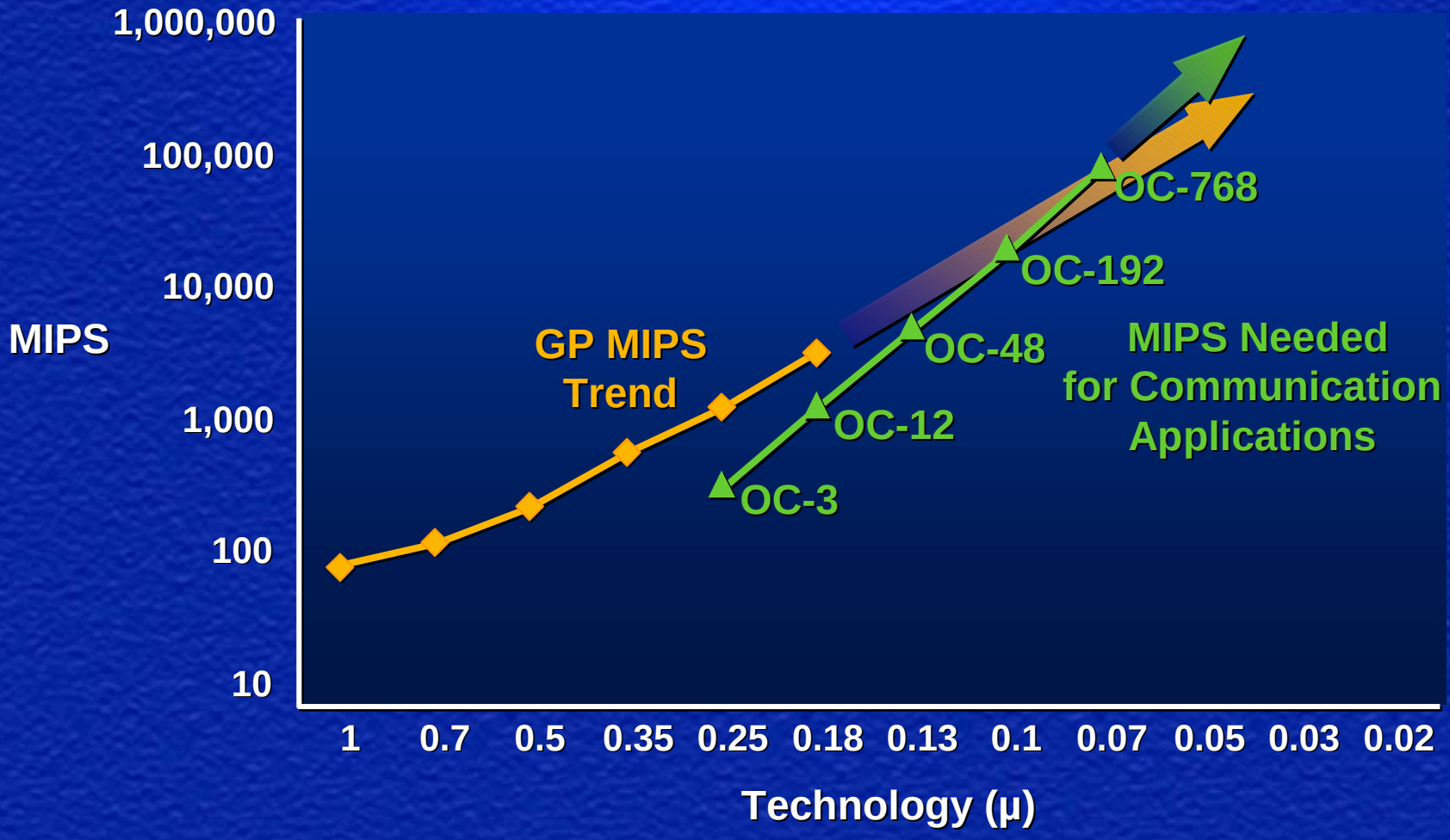
- **Virus scanning, security, easy attachments**
- **Embedded images, clips simultaneously**
- **Audio, speech**
- **Network Communication**
- **Encryption / Decryption**
- **Media Encode / Decode**

Today's Pentium 4:
3Ghz, 13k MIPs, 55M transistors

So what are we going to do with a billion transistors?

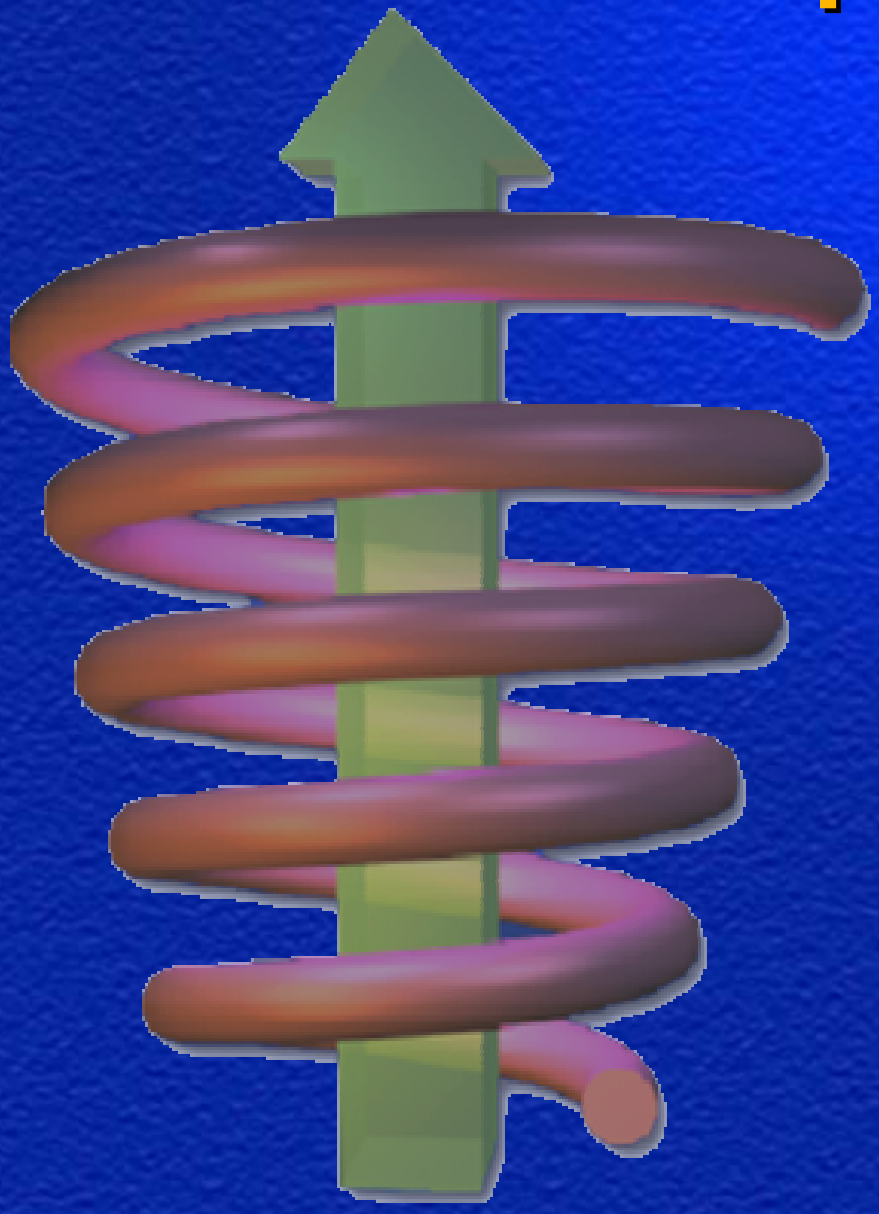
What is the next revolution of the digital spiral?

Communications Applications are Hungry…



…and Could Consume All Available MIPS

As the spiral turns … ..



Probabilistic computing

Wireless everything

Natural IO

Killer environment

Wireless Everything

Radios wherever they make sense!

Moore's law applied to spectrum

Foundation of Pervasive computing

Dependent on more MIPs for better digital computation & communication

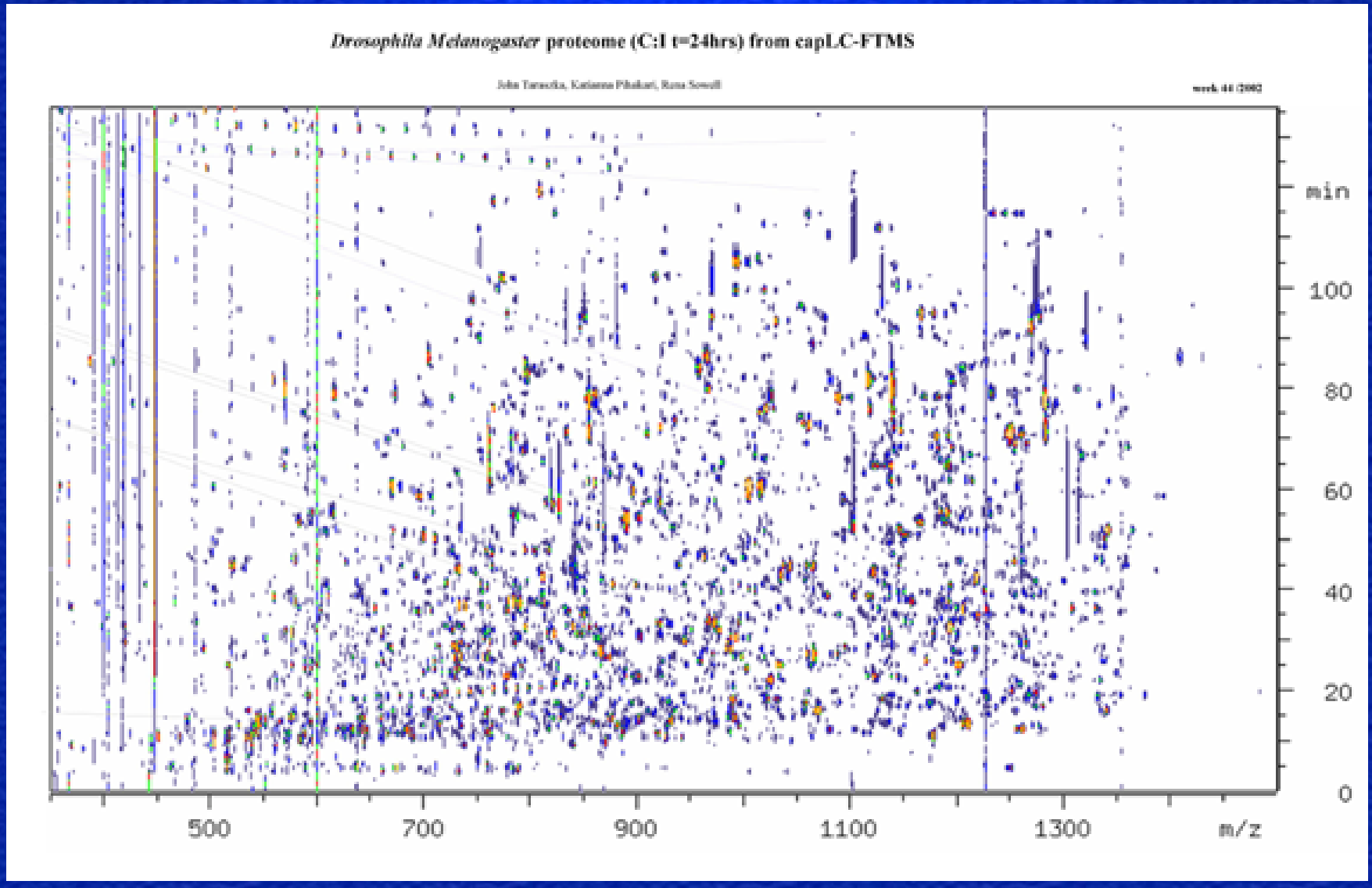
The digital spiral continues

Enter the next frontier

Processor Power Required

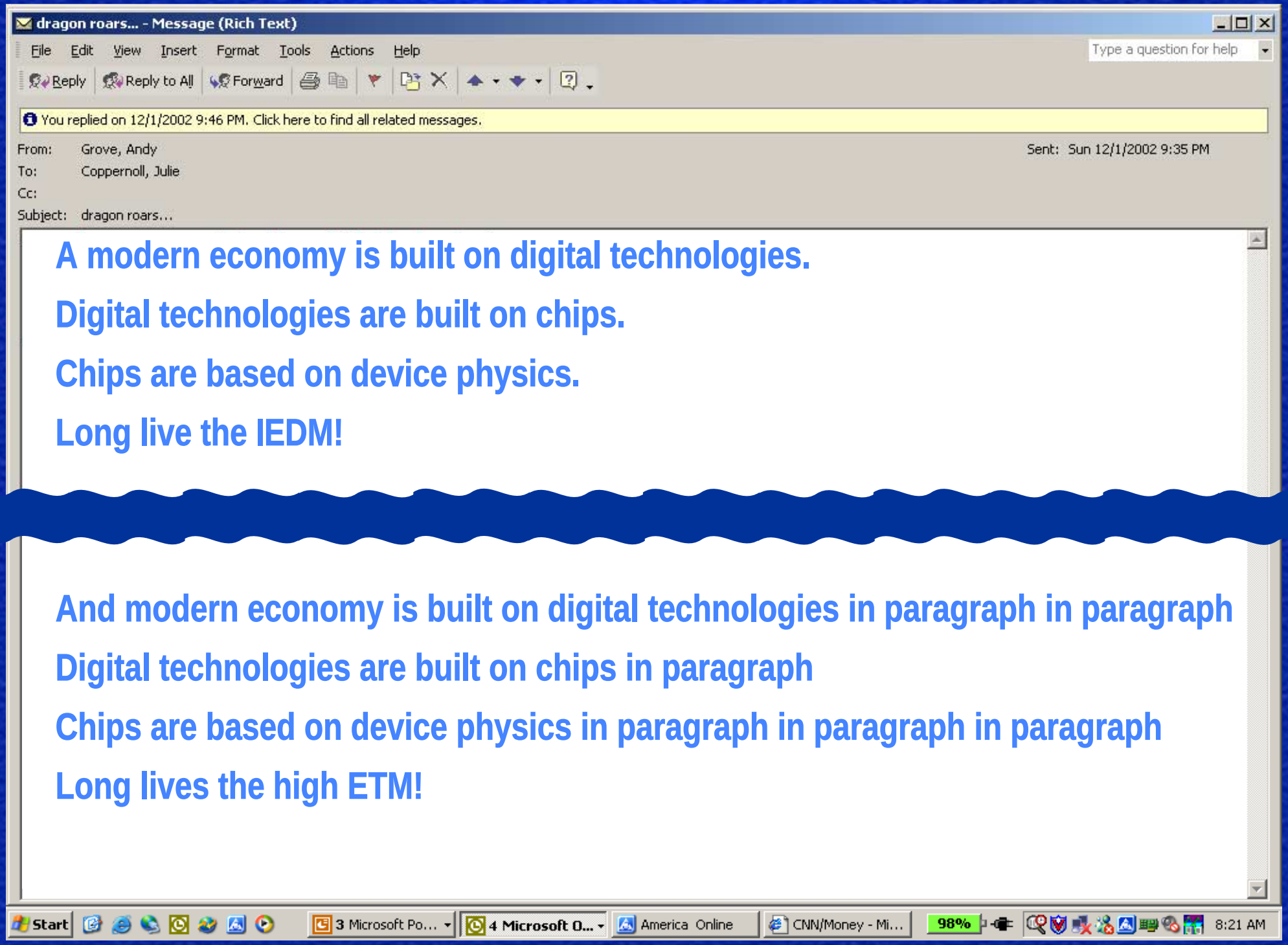
Intel®, Pentium®, 4 processor	1,099 MFLOPS
Speech to Text	1,500 MFLOPS
Natural Language Processing	6,550 MFLOPS
Feature Recognition	11,000 MFLOPS

Drosophila Melanogaster proteome



But first….

Get speech right!


dragon roars... - Message (Rich Text)
File Edit View Insert Format Tools Actions Help
Type a question for help
Reply Reply to All Forward
You replied on 12/1/2002 9:46 PM. Click here to find all related messages.
From: Grove, Andy
Sent: Sun 12/1/2002 9:35 PM
To: Coppernoll, Julie
Cc:
Subject: dragon roars...
A modern economy is built on digital technologies.
Digital technologies are built on chips.
Chips are based on device physics.
Long live the IEDM!
And modern economy is built on digital technologies in paragraph in paragraph
Digital technologies are built on chips in paragraph
Chips are based on device physics in paragraph in paragraph in paragraph
Long lives the high ETM!
Start
3 Microsoft Po...
4 Microsoft O...
America Online
CNN/Money - Mi...
98%
8:21 AM

We have a long way to go

Device Physics rules!